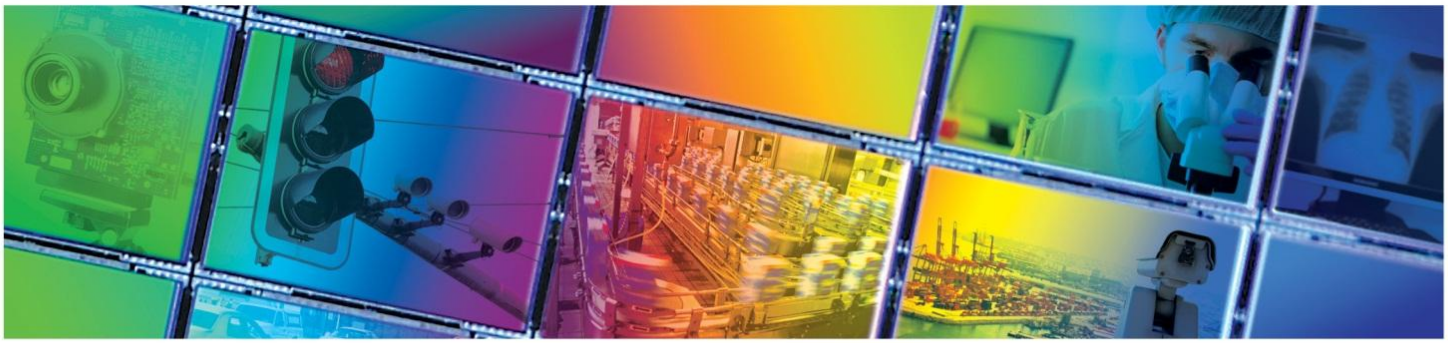
TRUESENSE
imaging, inc.

KAF-6303 IMAGE SENSOR

3072 (H) X 2048 (V) FULL FRAME CCD IMAGE SENSOR



JULY 27, 2012

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.0 PS-0039

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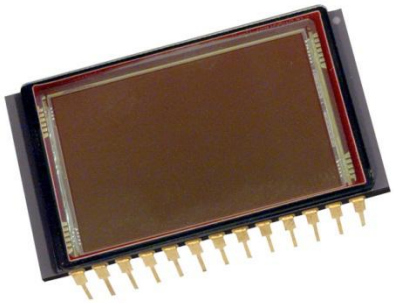
KAF-6303 Image Sensor



DESCRIPTION

The KAF-6303 Image Sensor is a high performance CCD (charge-coupled device) with 3072 (H) x 2048 (V) photo active pixels designed for a wide range of image sensing applications.

The sensor incorporates true two-phase CCD technology, simplifying the support circuits required to drive the sensor as well as reducing dark current without compromising charge capacity. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

FEATURES

- True Two Phase Full Frame Architecture
- TRUESENSE Transparent Gate Electrode for high sensitivity
- 100% Fill Factor
- Low Dark Current

APPLICATIONS

- Medical Imaging
- Scientific Imaging

Parameter	Typical Value
Architecture	Full Frame CCD
Total Number of Pixels	3088 (H) x 2056 (V)
Number of Active Pixels	3072 (H) x 2048 (V) = approx. 6.3 M
Pixel Size	9 µm (H) x 9 µm (V)
Active Image Size	27.65 mm (H) x 18.48 mm (V)
Chip Size	29.0 mm (H) x 19.1 mm (V)
Saturation Signal	100,000 electrons
Output Sensitivity	10 µV/electron
Quantum Efficiency (450, 550, 650 nm)	40%, 52%, 65%
Readout Noise (10 MHz)	15 electrons rms
Dark Current (T = 25 °C, Accumulation Mode)	<10pA/cm^2
Dark Current Doubling Rate	6 °C
Dynamic Range (Saturation Signal/Dark Noise)	76 dB
Maximum Data Rate	10 MHz
Package	CERDIP Package (sidebrazed)
Cover Glass	Clear or AR coated, 2 sides

Parameters above are specified at 25 °C, unless otherwise noted

Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H0703	KAF- 6303-AAA-CD-B2	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Grade 2	KAF-6303-AAA [Serial Number]
4H0704	KAF- 6303-AAA-CD-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0481	KAF- 6303-AAA-CP-B2	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Grade 2	
2H4478	KAF- 6303-AAA-CP-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Sample	
4H0079	KEK-4H0079-KAF-6303-12-5	Evaluation Board (Complete Kit)	N/A

See Application Note *Product Naming Convention* for a full description of the naming convention used for Truesense Imaging image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.
1964 Lake Avenue
Rochester, New York 14615

Phone: (585) 784-5500
E-mail: info@truesenseimaging.com

Truesense Imaging reserves the right to change any information contained herein without notice. All information furnished by Truesense Imaging is believed to be accurate.

Device Description

ARCHITECTURE

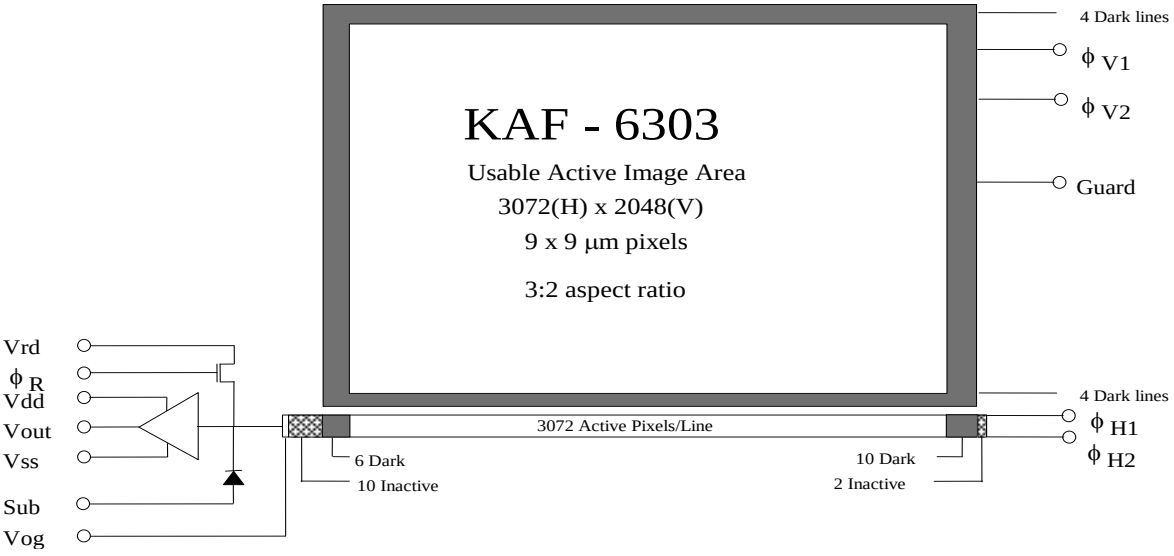


Figure 1: Block Diagram

The sensor consists of 3088 parallel (vertical) CCD shift registers each 2056 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The elements of these registers are arranged into a 3072 x 2048 photosensitive array surrounded by a light shielded dark reference of 16 columns and 8 rows. The parallel (vertical) CCD registers transfer the image one line at a time into a single 3100 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo-generated charge to a voltage for each pixel.

Dark Reference Pixels

Surrounding the peripheral of the device is a border of light shielded pixels. This includes 6 leading and 10 trailing pixels on every line excluding dummy pixels. There are also 4 full dark lines at the start of every frame and 4 full dark lines at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel, or the outer bounds of the chip (including the first two lines out), can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on FD. Once the signal has been sampled by the system electronics, the reset gate (φR) is clocked to remove the signal and FD is reset to the potential applied by Vrd. More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device. See Figure 2.

Dummy Pixels

Within the horizontal shift register are 10 leading and 2 trailing additional shift phases that are not associated with a column of pixels from the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions.

IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the φV1 and φV2 register clocks are held at a constant (low) level. See Figure 7.

CHARGE TRANSPORT

Referring again to Figure 7, the integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD's to the horizontal CCD register using the φV1 and φV2 register clocks. The horizontal CCD is presented a new line on the falling edge of φV2 while φH1 is held high. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the φH1 and φH2 pins in a complementary fashion. On each falling edge of φH2, a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

HORIZONTAL REGISTER

Output Structure

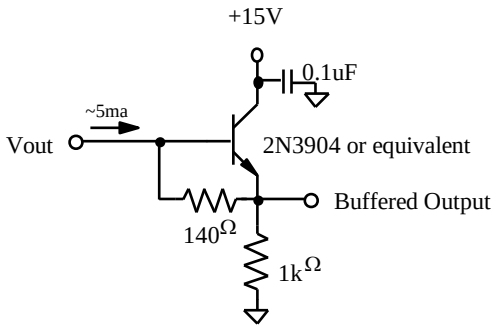


Figure 2: Output Structure Load Diagram

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

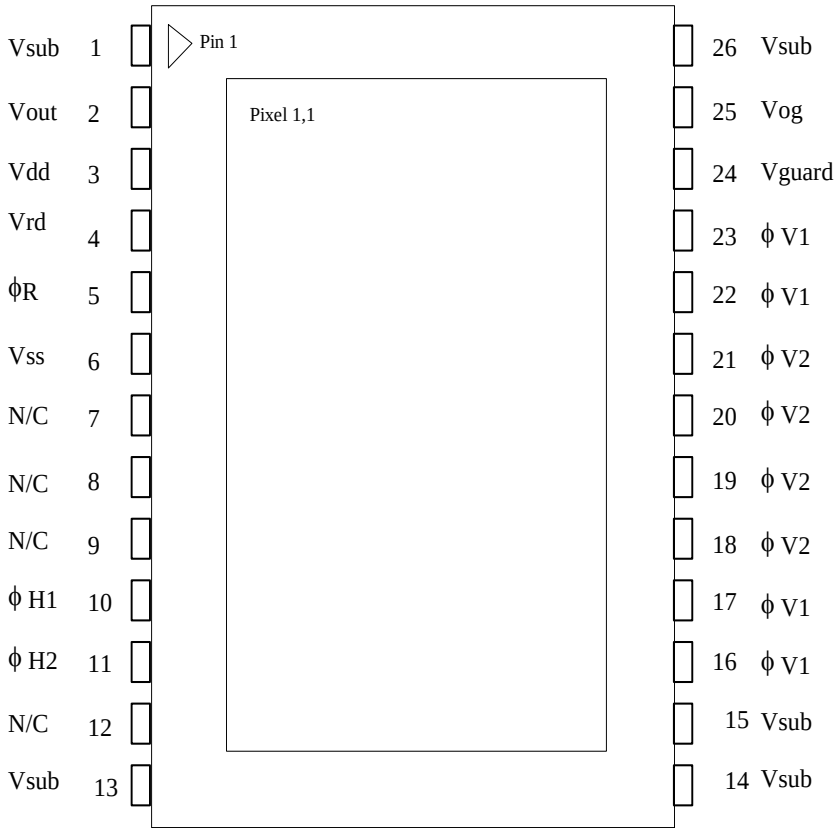


Figure 3: Pinout Diagram

Notes:

1. The KAF-1603 is mechanically the same and electrically identical to the KAF-0402 sensor. It is also mechanically the same as the KAF-0261 and KAF-3200 sensors, but there are some electrical differences since the KAF-0261 has two outputs and two additional clock inputs. The KAF-3200 requires that pin 11 be a “No connect” and be electrically floating. Refer to their specifications for details.

Pin	Name	Description
1	Vsub	Substrate (Ground)
2	Vout	Video Output
3	Vdd	Amplifier Supply
4	Vrd	Reset Drain
5	φR	Reset Clock
6	Vss	Amplifier Supply Return
7	N/C	No Connection (open pin)
8	N/C	No Connection (open pin)
9	N/C	No Connection (open pin)
10	φH1	Horizontal CCD Clock - Phase 1
11	φH2	Horizontal CCD Clock - Phase 2
12	N/C	No Connection (open pin)
13	Vsub	Substrate (Ground)

Pin	Name	Description
14	Vsub	Substrate (Ground)
15	Vsub	Substrate (Ground)
16	φV1	Vertical CCD Clock - Phase 1
17	φV1	Vertical CCD Clock - Phase 1
18	φV2	Vertical CCD Clock - Phase 2
19	φV2	Vertical CCD Clock - Phase 2
20	φV2	Vertical CCD Clock - Phase 2
21	φV2	Vertical CCD Clock - Phase 2
22	φV1	Vertical CCD Clock - Phase 1
23	φV1	Vertical CCD Clock - Phase 1
24	Vguard	Guard Ring
25	Vog	Output Gate
26	Vsub	Substrate (Ground)

Imaging Performance

Typical Operational Conditions

All values measured at 25 °C, and nominal operating conditions. These parameters exclude defective pixels.

Specifications

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Saturation Signal Vertical CCD capacity Horizontal CCD capacity Output Node capacity	Nsat	 85000 170000 190000	 100000 200000 220000	 120000 240000 240000	electrons / pixel	1	design[11]
Red Quantum Efficiency Green Quantum Efficiency Blue Quantum Efficiency	Rr Rg Rb	52 42 30	65 52 40	75 62 48	%QE		design[11]
Photoresponse Non-Linearity	PRNL		1.0	2.0	%	2	design[11]
Photoresponse Non-Uniformity	PRNU		1.0	3.0	%	3	die[10]
Dark Signal	Jdark		15 3.5	50 10	electrons / pixel / sec pA/cm^2	4	die[10]
Dark Signal Doubling Temperature		5	6.3	7.5	°C		design[11]
Dark Signal Non-Uniformity	DSNU		10	50	electrons / pixel / sec	5	die[10]
Dynamic Range	DR	70	76		dB	6	design[11]
Charge Transfer Efficiency	CTE	0.99997	0.99999				die[10]
Output Amplifier DC Offset	Vodc	9.5	10.5	11.5	V	7	die[10]
Output Amplifier Bandwidth	f-3dB		45		Mhz	8	design[11]
Output Amplifier Sensitivity	Vout/Ne$^-$	9	10	11	µV/e$^-$		design[11]
Output Amplifier output Impedance	Zout	175	200	2520	Ohms		design[11]
Noise Floor	ne$^-$		15	20	electrons	9	die[10]

Notes:

1. For pixel binning applications, electron capacity up to 330000 can be achieved with modified CCD inputs. Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
2. Worst-case deviation from straight line fit, between 1% and 90% of Vsat.
3. One Sigma deviation of a 128 x 128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25 °C.
5. Average dark signal of any of 12 x 8 blocks within the sensor (each block is 128 x 128 pixels).
6. 20log (Nsat / ne$^-$) at nominal operating frequency and 25 °C.
7. Video level offset with respect to ground.
8. Last output amplifier stage only. Assumes 10 pF off-chip load.
9. Output noise at 25 °C, nominal operating frequency, and tint = 0.
10. A parameter that is measured on every sensor during production testing.
11. A parameter that is quantified during the design verification activity.

Typical Performance Curves

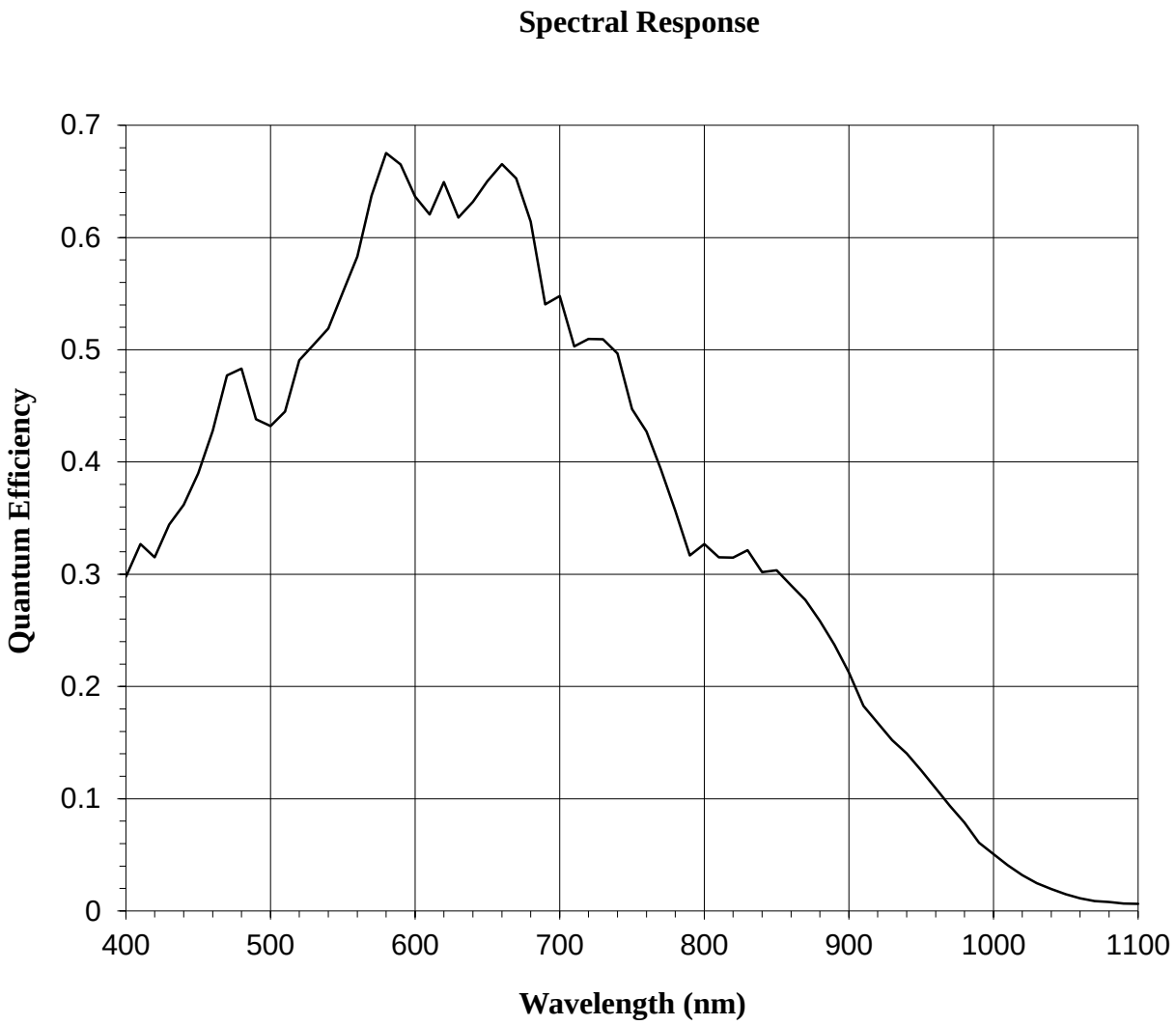


Figure 4: Typical Spectral Response

Defect Definitions

Operating Conditions

All defect tests performed at T = 25 °C

Specifications

Classification	Point Defect		Cluster Defect		Maximum Cluster Size	Column Defect	
	Total	Zone A	Total	Zone A		Total	Zone A
C2	≤90	≤45	≤36	≤18	5	0	0

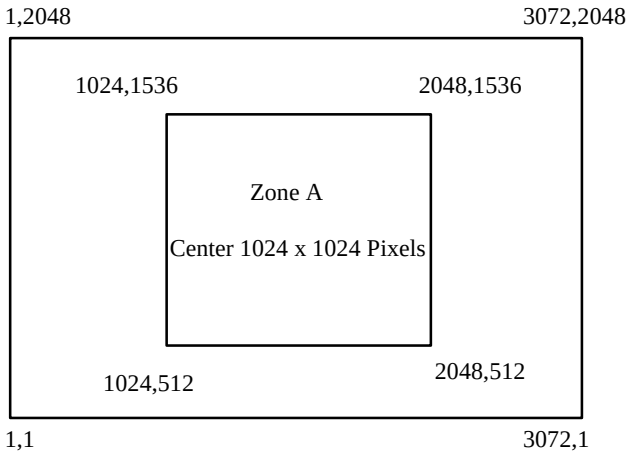


Figure 5: Active Pixel Region

Point Defects

Dark: A pixel that deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation.

-- OR --

Bright: A pixel with a dark current greater than 10,000 e^-/pixel/sec at 25 °C.

Cluster Defect

A grouping of not more than "Maximum Cluster Size" defects.

Column Defect

A grouping of >5 contiguous point defects along a single column.

A column containing a pixel with dark current > 30,000 e^-/pixel/sec, OR A column that does not meet the CTE specification for all exposures less than the specified Max sat. signal level and greater than 2 ke^-.

A pixel which loses more than 250 e^- under 2 ke^- illumination.

Neighboring Pixels

The surrounding 128 x 128 pixels or ± 64 column/rows.

Defect Separation

Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).

Defect Region Exclusion

Defect region excludes the outer two (2) rows and columns at each side/end of the sensor.

Operation

Absolute Maximum Ratings

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{diode}	0	20	V	1,2
Gate Pin Voltages - Type 1	V_{gate1}	-16	16	V	1,3
Gate Pin Voltages - Type 2	V_{gate2}	0	16	V	1,4
Inter-Gate Voltages	$V_{g\text{-}g}$		16	V	5
Output Bias Current	I_{out}		-10	mA	6
Output Load Capacitance	C_{load}		15	pF	6
Storage Temperature	T_{ST}	0	70	°C	
Humidity	RH	5	90	%	7

Notes:

1. Referenced to pin Vsub.
2. Includes pins: Vrd, Vdd, Vss, Vout, Vguard.
3. Includes pins: φV1, V2, H1, H2.
4. Includes pins: φR, Vog.
5. Voltage difference between overlapping gates. Includes: φV1 to V2, H1 to H2, V2 to H1, H2 to Vog.
6. Avoid shorting output pins to ground or any low impedance source during operation.
7. T = 25 °C. Excessive humidity will degrade MTTF.

DC Bias Operating Conditions

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	Vrd	10.5	11.0	11.5	V	0.01	
Output Amplifier Return	Vss	1.5	2.0	2.5	V	0.45	
Output Amplifier Supply	Vdd	14.5	15	15.5	V	Iout	
Substrate	Vsub	0	0	0	V	0.01	
Output Gate	Vog	3.75	4.0	5.0	V	0.01	
Guard Ring	Vlg	8.0	10.0	12.0	V	0.01	
Video Output Current	Iout		-5	-10	mA	-	1

Notes:
1. An output load sink must be applied to Vout to activate output amplifier – see Figure 2.

AC Operating Conditions

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance
Vertical CCD Clock - Phase 1	φV1	Low	-10.5	-10.0	-9.5	V	82 nf (all φV1 pins)
Vertical CCD Clock - Phase 1	φV1	High	0.5	1.0	1.5	V	82 nf (all φV1 pins)
Vertical CCD Clock - Phase 2	φV2	Low	-10.5	-10.0	-9.5	V	820 nf (all φV2 pins)
Vertical CCD Clock - Phase 2	φV2	High	0.5	1.0	1.5	V	820 nf (all φV2 pins)
Horizontal CCD Clock - Phase 1	φH1	Low	-6.0	-3.0	-3.0	V	400 pF
Horizontal CCD Clock - Phase 1	φH1	High	4.0	7.0	7.0	V	400 pF
Horizontal CCD Clock - Phase 2	φH2	Low	-6.0	-3.0	-3.0	V	400 pF
Horizontal CCD Clock - Phase 2	φH2	High	4.0	7.0	7.0	V	400 pF
Reset Clock	φR	Low	-4.0	-3.0	-2.0	V	10 pF
Reset Clock	φR	High	3.5	4.0	5.0	V	10 pF

Notes:
1. All pins draw less than 10 µA DC current.
2. Capacitance values relative to VSUB.

Timing

Requirements and Characteristics

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
φH1, φH2 Clock Frequency	f_H		4	15	MHz	1, 2, 3
φV1, φV2 Clock Frequency	F_V		25	50	kz	1, 2, 3
Pixel Period (I count)	t_e	67	250		ns	
φH1, φH2 Setup Time	$t_{\phi HS}$	0.5	1		µs	
φV1, φV2 Clock Pulse Width	$t_{\phi V}$	10	20		µs	2
Reset Clock Pulse Width	$t_{\phi R}$	10	20		ns	4
Readout Time	$t_{readout}$	531	1719		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	258.2	836		µs	7

Notes:

1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5 - 10% of clock period. Cross-over of register clocks should be between 40 - 60% of amplitude.
4. φR should be clocked continuously.
5. $t_{readout} = (2056 * t_{line})$.
6. Integration time is user specified. Longer integration times will degrade noise performance.
7. $t_{line} = (3* t_{\phi V}) + t_{\phi HS} + (3100) + t_e$.

FRAME TIMING

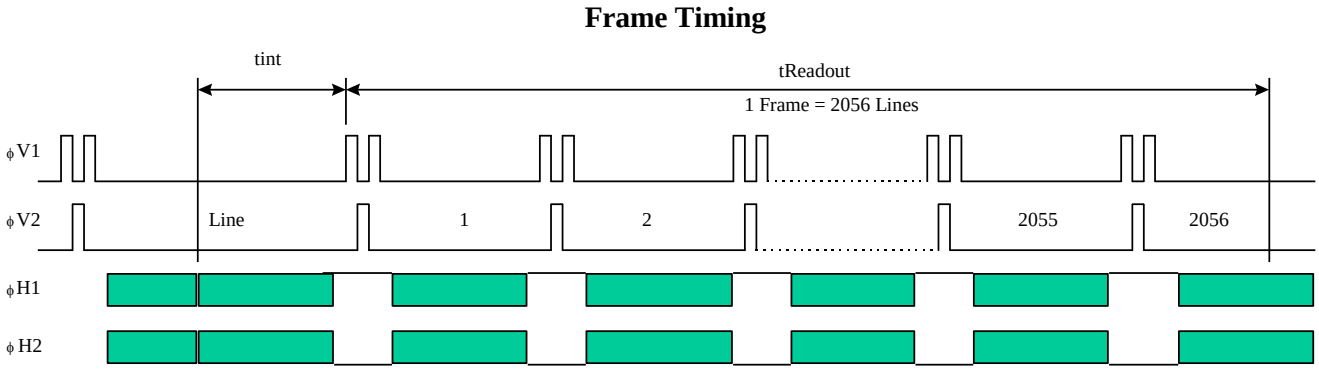


Figure 6: Frame Timing

LINE TIMING (EACH OUTPUT)

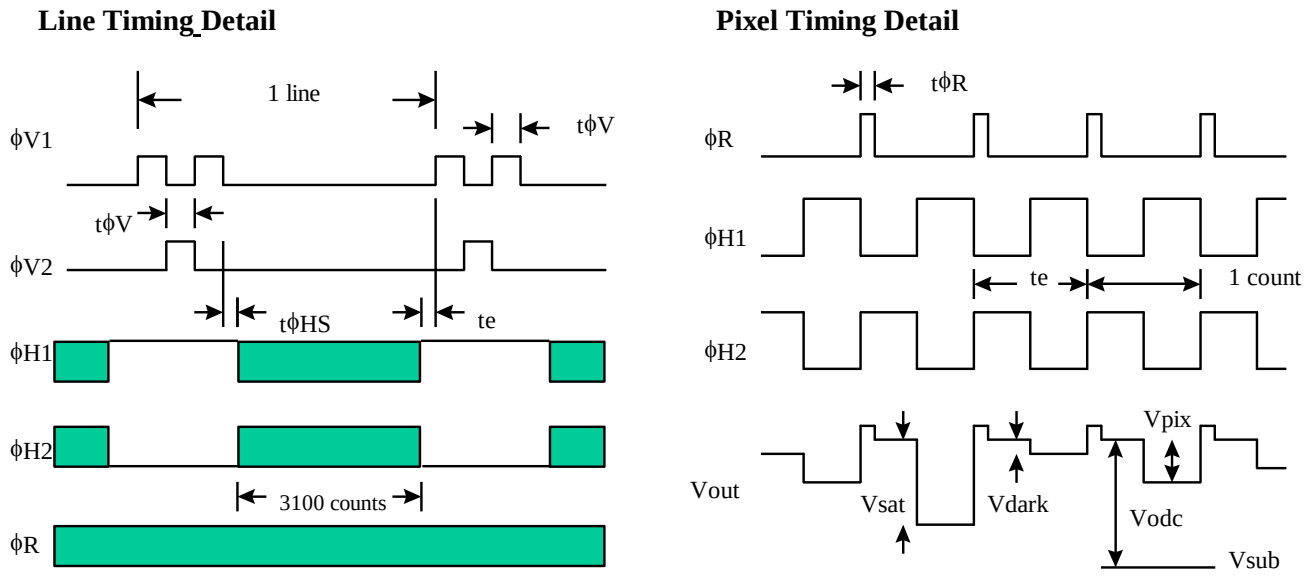
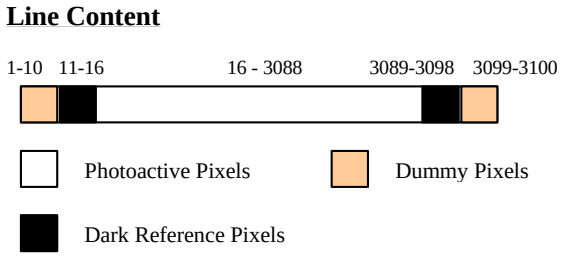


Figure 7: Line Timing



Vsat	Saturated pixel video output signal
Vdark	Video output signal in no light situation, not zero due to Jdark
Vpix	Pixel video output signal level, more electrons =more negative'
Vodc	Video level offset with respect to vsub
Vsub	Analog Ground

* See Image Aquisition section (page 4)

Figure 8: Timing Diagrams

Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	0	70	°C	1
Operating Temperature	T_{OP}	-60	60	°C	

Notes:
1. Storage toward the maximum temperature will accelerate color filter degradation.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Information

COMPLETED ASSEMBLY

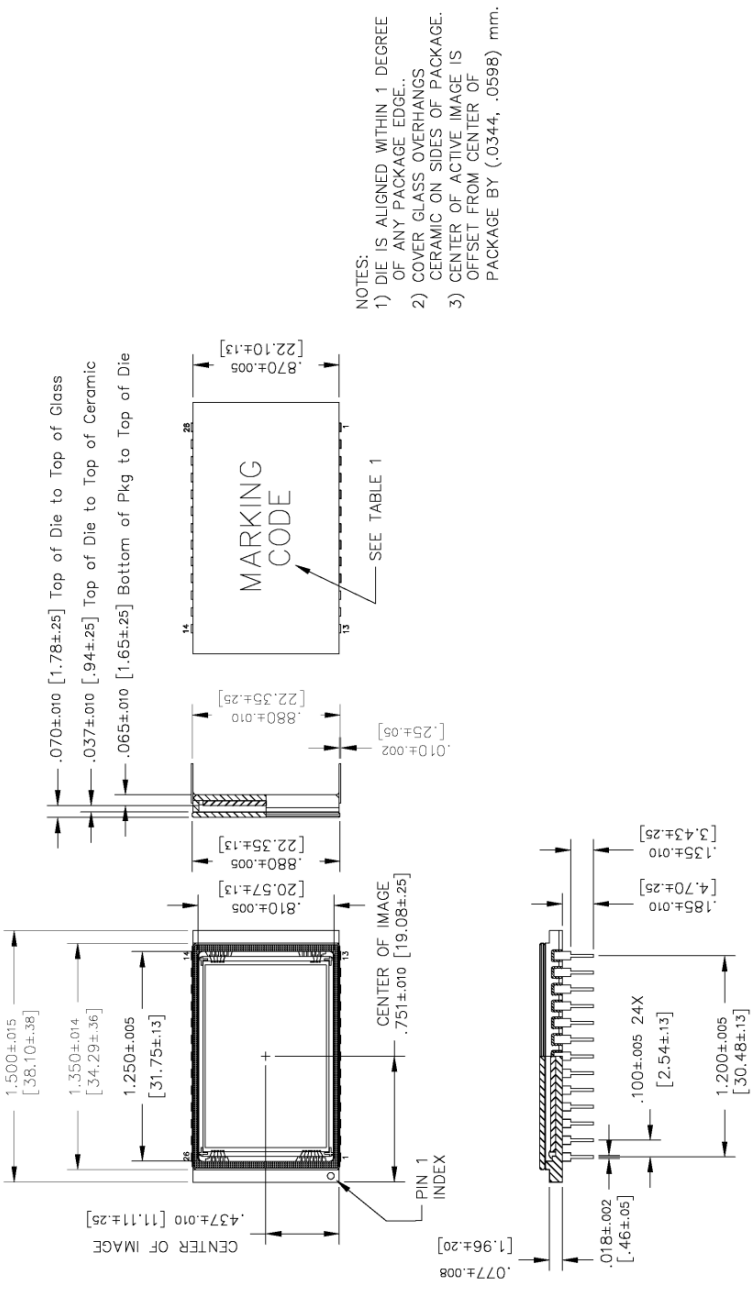


Figure 9: Completed Assembly (1 of 2)

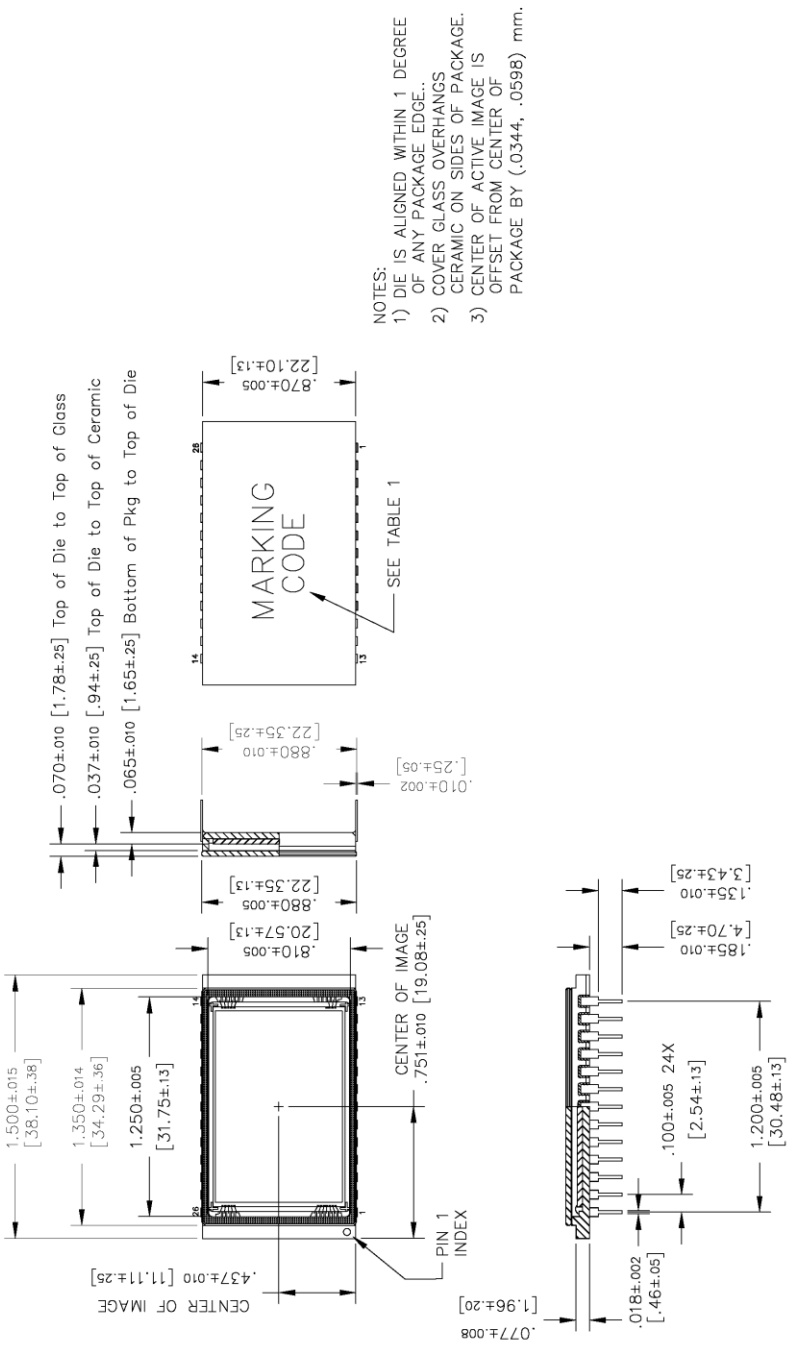


Figure 10: Completed Assembly (2 of 2)

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from Truesense Imaging upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

Truesense Imaging reserves the right to change any information contained herein without notice. All information furnished by Truesense Imaging is believed to be accurate.

Life Support Applications Policy

Truesense Imaging image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of Truesense Imaging, Inc.

Revision Changes

MTD/PS-0207

Revision Number	Description of Changes
1.0	• Initial Release.
	• Revised class 1 cosmetic specification. • Removed UV enhanced device. • Resubmitted for Cluster correction and definition.

2.0	• Section 4.3 Cosmetic Specification:
	  ○ Remove Class 3
	  ○ Revise Class 2 as follows:
	  ▪ Point Defects: Total 90, Zone A 45
	  ▪ Clusters: Total 36, Zone A 18
	  ▪ Columns Total 0
	• Section 5.1 Quality and Reliability, updated.

3.0	• Section 3.3 AC Operating Conditions:
	  ○ Change Horizontal CCD Clock voltages for Phase 1 and Phase 2 as follows:
	  ▪ Low Nominal from –4.0 to –3.0 V
	  ▪ Low Max. from –3.5 to –3.0 V
	  ▪ High Nominal from 6.0 to 7.0 V
	  ▪ High Max. from 6.5 to 7.0 V
	• Resubmission change:
	  ○ Corrected V1, V2 Clock Capacitance form 820 to 82 nF.
	  ○ Updated ESD Caution.

4.0	• Updated format. Removed part numbers
4.1	• Replaced photo of KAF-6303 device
4.2	• Removed Class 1 parts from the defect specification table
4.3	• Corrected Total number of pixels from 1.6 M to 6.3 M

PS-0039

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections • Corrected Nominal Dynamic range shown in Imaging Performance section to be consistent with correct value shown in Summary Specifications table